Solder Joints Quality Assessment as Function of VPS Process Parameters

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*The challenges for the companies involved in conception, development and/or manufacturing of electronic products are the lead-free technology with its increased melting temperature of the solder alloy and trend to reduce the solder materials cost by usage of lead-free solder pastes with low or no silver content. Defining the elements ***P**ad-**P**aste-**P**in-**P**rocess* as Key Process Input Variables (KPIV) in terms of ****4P Soldering Model**** *concept, the solder joints are the result of KPIV synergistically interactions and correlations, with consequences over their microstructure. In the paper, taking into consideration the cooling rate influence over intermetallic compounds formation and microstructure, the investigations over electrical and mechanical properties of solder joints resulted from Vapour Phase Soldering (VPS) process in terms of 4P Soldering Model are presented. Maintaining the pad and pin elements of KPIV as references, the solder joints properties determined by low silver content pastes usage as function of cooling rate parameters of VPS process were studied. The results of the studies performed and presented in the paper will be used for improving process control in order to minimize losses on VPS lines, to reduce defects numbers and re-work time.*

Keywords: Shape memory alloy (SMA), Phase transformation temperature, NiTi precipitates, Differential scanning calorimetry (DSC)

In present the goal of the companies involved in conception, development and/or manufacturing of electronic products is to assure maximum assembling quality with minimum costs, in reduced time to market condition. These tasks require the assembling process control and optimization in order to reduce the number of technological procedures, minimizing losses on technological lines, reducing defects number and re-work time. In the assembling zone, the quality of the electronic module strongly depends on the functionality of its interconnection structure realized at the surface of the printed circuits board (PCB) by solder joints as result of soldering process. The challenges are the lead-free technology with its increased melting temperature of the solder alloy, a real turning point in the Surface Mount Technology (SMT) which has been defined by the RoHS Directive appearance [1, 2]. The answer is offered by the renaissances of the Vapour Phase Soldering (VPS) technology that becomes to be taken into consideration because of its high efficiency and uniform heating characteristics in an oxygen free environment (heat transfer coefficient is about 100 to 400W/m^{2}K in condensation in compare with maximum 60 W/m^{2}K at peak temperature profile in radiation and only 5 W/m^{2}K in convection) [3].

The solder joints are responsible for electrical continuity, heat conduction, and mechanical attachment, all these specific functions (mechanical, thermal and electrical) being determined by their microstructure, especially the intermetallic layer.

In order to realize the assessment of the solder joints quality as function of vapour phase soldering process parameters, the authors optimized the VPS thermal profile using the facilities offered by IBL SLC309 [4] equipment and studies were performed regarding functionality of solder joints resulted by using solder pastes with low or no silver content as function of cooling rate parameters of VPS process.

Analyzing the solder joint quality from his functionality point of view, the influence of the solder fillet shape and of the mechanical properties at the interface between the solder joint, the component lead and the pad over the strength of the solder joint could be noticed. Also, the reflow soldering thermal profile (TP) has a great impact on solder joint performance since it influences his microstructure. In conclusion, we can identify elements that have a major influence on solder joint functionality as practical elements contributing to the soldering process: the component terminal (pin), the pad and the solder paste, the solder joint being the result of the reflow soldering process (RSP) temperature gradient action over the trinomial solder **P**aste, electronic components terminals/**P**in and PCBs **P**ads. Consequently the solder joints quality can be correctly evaluated taking into consideration not only the severally intrinsic parameters of the trinomial elements, **P**ad-**P**aste-**P**in, but also interrelate the complex reaction at the interface between them in interdependence with the RSP parameters. Defining the complex elements **P**ad-**P**aste-**P**in-**P**rocess as Key Process Input Variables (KPIV), the solder joints can be considered in terms of **4P Soldering Model** concept [5], the result of KPIV synergistically interactions and correlations, with consequences over their microstructure.

Considering the conception and design stages of the life cycle of an electronic product (PLC) the morphological structure of **4P Soldering Model** concept (Fig.1) can be defined. The manufacturing process for an electronic product is developed according with a dedicated project, result of Design for Manufacturing (DfM) process.

DfM process can be defined as a space of the possible design solutions, D_i, being conditioned by marketing, business line, available manufacturing technologies, test, delivery and finally sale requirements.

Corresponding to D_i solutions in the project will be defined the electronic components and PCBs design where will be defined the pads according with electronic components

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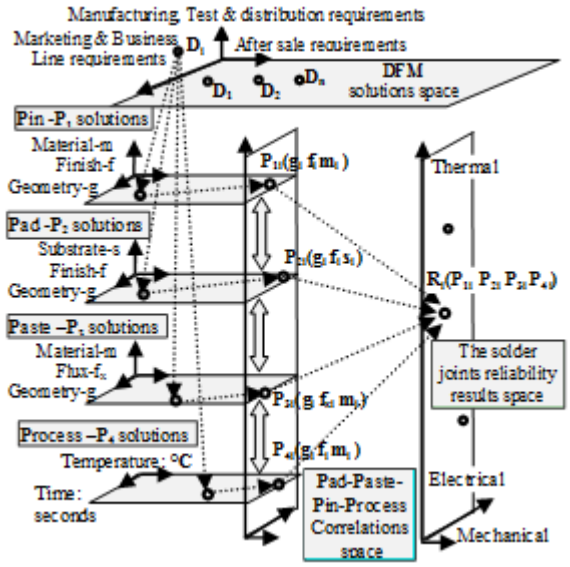

Fig. 1 4P Soldering Model morphological structure

footprints. Taking into considerations the SMC terminals as pins can be defined a space of the possible **P**in solutions, $\mathbf{P_1}$, being conditioned by the pin material (copper), finish (Sn, Ni, NiPdAu, according to JESD97 / IPC 1066 Standards) [6] and geometry (thickness and forms: pin, win gull, balls, according to IPC7351) [7]. For pads there will be two major elements, metallic surface as support of solder joint, characterized by geometry and finishes (Electroless Nickel Immersion Gold (ENIG); Chemical Tin (ChTin); Hot Air Surface Leveling (HASL - SnCuNi); Organic Solderability Preservative (OSP) Immersion Silver (ImmAg); Copper without finishes and substrate, with important contribution over thermal mass and thermal transfer, consisting of different type of PCBs core materials and geometry. As consequence, the space of the possible **P**ad solutions, $\mathbf{P_2}$, can be defined, being conditioned by the pad finishes, geometry and substrate.

In the manufacturing area, according with design solutions and requirements imposed by **P**in and **P**ad solutions, solder paste will be selected from a typically **P**aste solutions space $\mathbf{P_3}$ determined by solder alloy type as basic material, flux and geometry aspects consequences of stencil design determinate by printing requirements.

Typically for RSP in SMT, the key issue is the heat transfer control in order to realize the optimum thermal profile (TP). The TPs analyzes are based on recommendations of IPC/ JEDEC J-STD-020C standard [8]. As a consequence, a space temperature / time, for reflow soldering **P**rocess solutions, $\mathbf{P_4}$, can be defined. The different RSP are characterized by different TPs as function of used soldering technology.

The **P**ads having different finishes (NiAu, ImmAg, ImmSn, HASL, OSP) and geometry, realized on PCBs having different core material, (FR4, glass, Al, Cu, Al_2O_3), the components terminals/**P**ins/balls having different finishes, material and geometry, the different solder **P**aste type, having different solder material, flux and geometry, the reflow soldering **P**rocess with their typically TPs are the **4P Soldering Model** variables.

The projections of D_i (DfM proposed solution) to **P**in-**P**ad-**P**aste-**P**rocess possible solutions spaces will generate proposed solutions for each of KPIV.

Defining **The Pad-Paste-Pin-Process Correlations Space**, as a space of synergistically interactions and correlations between KPIV proposed solutions projections, the result will be final solutions for **P**in-**P**ad-**P**aste-**P**rocess as **4P Soldering Model** KPIV, having as univocally application in **The Solder Joints Reliability Results Space** characterized by the reliability function R:

$$R = R_i\ (P_{1i}, P_{2i}, P_{3i}, P_{4i}) \qquad (1)$$

where: $P_1 = P_{1i}\ (g_i f_i m_i)$ represent Pin functions; $P_2 = P_{2i}\ (g_i f_i s_i)$ represent Pad function; $P_3 = P_{3i}\ (g_i f_{xi} m_i)$ represent Paste function; $P_4 = P_{4i}\ (T,t)$ represent Process function

With: g_i =geometry; f_i =finish; m_i =material; s_i =substrate; f_{xi} =flux; T =temperature; t =time.

Experimental part

The experiments were determined by extending the use of VPS technology [9] and have been designed taking into account these practical requirements:

A. Optimizing the thermal profile for the VPS in order to ensure the conditions of production with zero defects;

B. Introduction in manufacturing of solder pastes with low or no silver content in order to reduce production costs by lowering costs for soldering materials, maintaining or improving quality in assembly with reference solder pastes based on lead-free solder alloy SAC305 type.

Designing of the PCBs test necessary for conducting experiments were realized on the basis of requirements and constraints generated by these initial requirements and completed in accordance with the 4P Soldering Model proposed concept. The test PCBs were assembled under similar conditions to those in manufacturing from the economic environment in order to assure solders joints quality assessment and functionality. In consequence, two types of test boards were designed, each of them having a serial electrical circuit, type *daisy chain*, used for interconnect chip resistors. These circuits allow checking of electrical function by measuring the voltage drop over series electrical resistance of the solder joint and chip resistor using in four-point measurement method. In order to determine the electrical resistance values of the solder joints were used different chip resistors with nominal value of zero ohms having different packages. One of the PCB test type, P2, was made with 10 chip resistors type 2512 and finish type ENIG for pads. The other board, P1, was made with 11 chip resistors 1206 type and 15 for each 0603 respectively 0402 types, with three types of finishes (F) for pads: HASL (F1), OSP (F2) and ENIG (F3). On PCB test P1 type was made an asymmetric interconnection structure for some pads of 1206 chip resistors type in order to verify the VPS thermal profile capability to not cause tombstoning (fig.2).

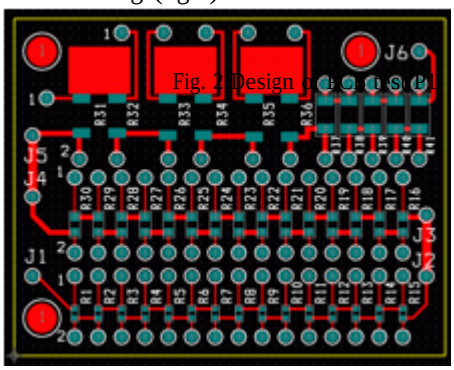

Fig. 2 Design of PCB test P1

To assemble P1, stencils have been designed with thicknesses of 100 and 120 microns, three types of thermal profiles for the VPS and five types of solder pastes (SP) were considered: SN100C (SP1) without silver content, SN100C-XF3 (SP2) and SACX0807 (SP3) with low content of silver and SACX0307 (SP4). The paste type OM338T SAC305 (SP5) was used as reference. In order to cover the experiments, 90 test boards with the base material FR-4,

1.6mm thickness and dimensions: 46 x 36 mm were carried out.

It was designed a thermal profile to provide a rate of heating up to 3 °C/s for preheating up to a plateau of about 150 °C and less than 1 °C/s over 200 °C, in order to eliminate defects such tombstoning and wicking. Differentiation between VPS thermal profiles were determined by the cooling rate under 0.5 °C/s, profile *Slow* (P40), about 1.5 °C/s for the profile *Normal* (P39) and about 4 °C/s, profile *Fast* (P37).

The *Printing* was done manually using laser cut stainless steel stencils, on a LPKF and the *Placement* was done also manually using a DIMA Pick-and-Place SMFL-3000. For *Reflow* was used IBL equipment SLC309.

Assembled test boards were coded *Stencil / Paste / Pad Finishes / Resistor houses*, using the above notation.

Two groups of 45 test boards P1 were created according to the printing stencil used, S1 respectively S2. Each group of P1 boards having F1-F3 pad finishes were printed with each of the SP1-SP5 solder pastes and soldered using profiles P37, P39 and P40 (fig. 3).

In order to check the mechanical function of the solder joints, shear tests were done, using the multifunctional bond tester *Condor 70-3*, with capability of 40kgf maximum

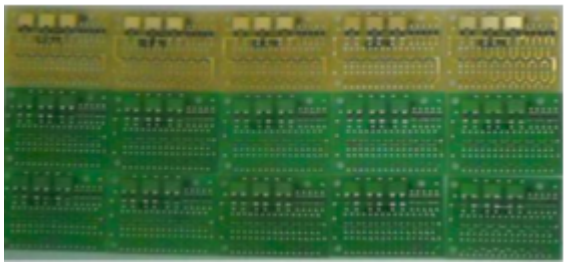

Fig. 3 Test boards P1, assembled with one type of VPS TP

shear force, possibilities to measure the maximum force and to take the imagines from process in real time.

The experiments offer the possibility to appreciate and compare the influence of paste and VPS process over electrical and mechanical functions of solder joints in terms of 4P Soldering Model. The following situations could be identified: The solder pastes types influences when is used the same thermal profile:

$$R = R_i(P_{3i}),\ P_{1i},P_{2i},P_{4i} = \text{constant} \quad (2)$$

The process influences using the slow, normal and fast thermal profile (P37, P39, P40) in order to assembly P1

No Crt	P	SP	F	S1			S2		
				R1206	R0603	R0402	R1206	R0603	R0402
1	P37	SP1	F1	0.78	1.68	0.91	0.69	4.43	0.88
2		SP2	F1	1.14	1.57	1.31	0.79	4.48	0.98
3		SP3	F1	0.85	1.04	0.79	0.67	4.61	0.79
4		SP4	F1	0.95	1.17	1.41	0.73	4.20	1.09
5		SP5	F1	0.71	1.03	0.88	0.55	4.06	0.46
6		SP1	F2	1.04	2.13	0.97	0.78	4.63	0.89
7		SP2	F2	1.20	1.98	1.23	0.83	4.91	0.96
8		SP3	F2	1.04	1.73	1.04	1.01	4.86	1.13
9		SP4	F2	1.08	1.70	1.44	0.72	4.67	1.23
10		SP5	F2	0.90	1.67	1.06	1.00	4.65	1.24
11		SP1	F3	1.03	2.18	1.53	1.14	5.55	1.41
12		SP2	F3	1.14	2.01	1.63	1.20	5.29	1.56
13		SP3	F3	0.96	1.87	1.65	0.95	4.88	1.58
14		SP4	F3	1.06	2.15	1.54	0.89	5.18	1.56
15		SP5	F3	0.90	1.72	1.41	0.88	4.93	1.66
16	P39	SP1	F1	0.78	1.31	0.90	0.89	4.41	1.08
17		SP2	F1	0.88	1.40	1.22	0.74	4.41	0.63
18		SP3	F1	0.80	1.44	1.13	0.58	4.42	0.67
19		SP4	F1	0.73	1.47	1.31	0.78	4.17	0.68
20		SP5	F1	0.88	1.30	1.02	0.66	4.30	0.88
21		SP1	F2	0.73	1.08	1.05	0.89	4.99	0.79
22		SP2	F2	1.06	1.36	0.73	0.75	4.77	1.17
23		SP3	F2	0.62	1.21	1.01	0.81	4.61	1.02
24		SP4	F2	0.84	1.21	1.05	0.82	4.44	1.11
25		SP5	F2	0.81	1.45	1.38	0.68	4.76	1.08
26		SP1	F3	1.21	2.34	1.40	1.40	5.30	1.63
27		SP2	F3	1.15	2.56	1.92	1.20	5.02	1.75
28		SP3	F3	1.20	2.50	1.85	1.12	5.33	2.13
29		SP4	F3	1.31	2.32	2.07	1.08	5.29	2.04
30		SP5	F3	1.24	2.26	2.34	0.99	5.18	1.84
31	P40	SP1	F1	1.18	4.82	0.93	0.90	4.98	0.85
32		SP2	F1	1.13	5.12	0.99	0.86	4.72	0.57
33		SP3	F1	0.74	4.98	1.20	0.66	4.47	0.82
34		SP4	F1	0.82	4.84	1.20	0.76	4.53	0.83
35		SP5	F1	0.83	1.31	1.17	0.78	4.13	0.80
36		SP1	F2	1.18	4.87	1.27	0.84	4.77	0.90
37		SP2	F2	0.79	4.78	1.16	1.17	4.98	1.15
38		SP3	F2	0.52	4.48	0.90	0.76	4.80	1.01
39		SP4	F2	0.81	4.96	1.12	0.79	4.76	0.93
40		SP5	F2	0.53	1.18	1.31	0.85	4.60	0.84
41		SP1	F3	1.54	5.64	2.50	1.32	5.31	2.06
42		SP2	F3	1.24	5.31	2.45	1.14	5.17	1.36
43		SP3	F3	1.03	5.48	2.03	1.25	5.63	1.85
44		SP4	F3	1.43	5.61	2.12	1.24	5.36	1.77
45		SP5	F3	1.41	3.58	1.90	1.21	5.29	1.78

Table 1
SOLDER JOINTS RESISTANCES AS FUNCTION OF SOLDER PASTE AND VPS PROFILE

test boards with each of solder paste (SP1-SP5):

$$R = R_i(P_{4i}),\ P_{1i},P_{2i},P_{3i} = \text{constan} \quad (3)$$

Results and discussions

The experiments were started with trials for optimization of the VPS process thermal profile (TP) in order to fix the *Fast, Normal* and *Slow* profile according with imposed value (fig.4).

The thermal profiles were optimized in order to avoid tombstoning at resistors R31-R36 taking into account the specific design (fig.4).

The electrical functions were tested using a serial electrical circuit realized with all board P1 from a group, which assured the same constant current value in all daisy chain, practical for all tested solder joints. The drop of electrical tension between testing points, proportional with the electrical resistance of two solder joints and one 0&! chip resistor was measured for 1.0 A constant current using four points' method. The electrical measurement values (resistances) as function of solder paste and VPS thermal profile are present in table 1. The results represent the value of equivalent resistance between the test points.

The average value could be considered specific for each of the soldering process according with used thermal profile, stencil, pad finishes and paste. In the same test could be measured directly on chip resistor the drop of electrical tension and indirect, taking into account the constant current, the resistor real resistance value. The average resistance values measured for each of resistors types are: 13.45mΩ for R1206, 19.37 mΩfor R0603 and 16.41 mΩ for R0402.

Shear tests were processed with Condor 70-3 software for SN100C and SAC305 alloys, corresponding to solder paste used in the experiments SP1 and SP5.

Figure 5 presents the system which corresponds to the real shear test applied over solder joints.

The main force was applied on the contact surface between machine nail and electronic component, having a ramped form. Considering as reference SAC305 solder paste (SP5), it could be noticed that the SN100C (SP1) solder paste proved lower shear force mean values for any given pad finishes (F1, F2 and F3), regardless the thermal profile, type of chip case (0402, 0603 and 1206), or stencil thickness (S1 and S2).

In table 2 are the mean values for shear force for S1 and 0603 chip case, for different pad finishes and TD. SP1 and SP5 shear force mean values for S1stencil, 0603 chip case and F3 pad finish, for different TP (P37, P39 and P40) are compare in figure 6.

Comparative studies of shear tests with the solder joint stereo micro fractography were done on S2 stencil type, using SP1 and SP5 solder paste, on F3 PCB pad finish, at two thermal profiles, fast (P37) and slow (P40).

The samples were studied at both fractures sides, in concordance with figure 7, in order to correlate the stress graph with the fracture type. In all micro fractography appears an intercrystalline stretch combine with torsion failure and in lower once appears a squeeze combine also

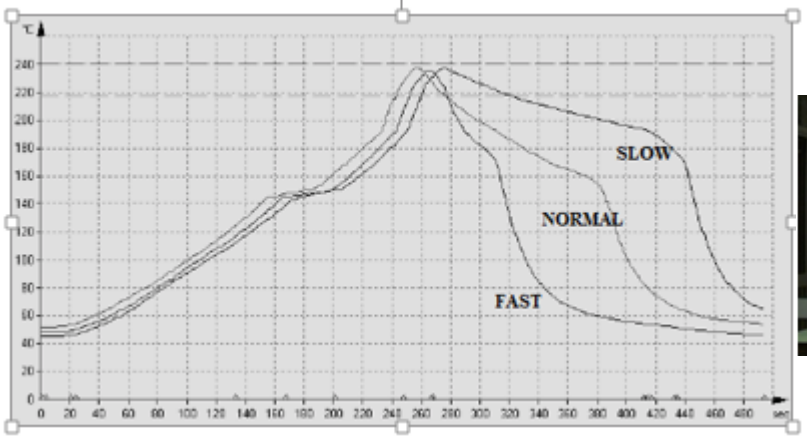

Fig. 4 VPS thermal profile

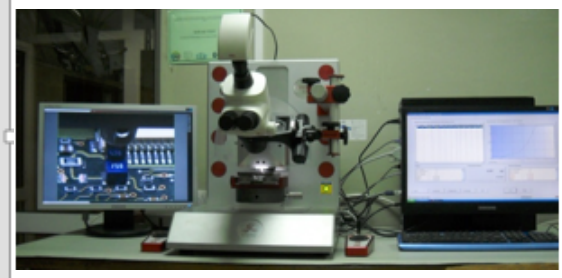

Fig. 5 The multifunctional bond tester *Condor 70-3*

Table 2

SHEAR FORCE MEAN VALUES FOR S1 AND 0603 CHIP CASE, F1, F2, F3 PAD FINISHES FOR DIFFERENT TP

Thermal profile	Pad finish	Alloy type	Shear force, [kgf]
P 37 (Fast)	F1	SP1	3.11
		SP5	3.31
	F2	SP1	2.90
		SP5	2.98
	F3	SP1	2.23
		SP5	2.86
P 39 (Normal)	F1	SP1	2.92
		SP5	3.61
	F2	SP1	2.94
		SP5	3.60
	F3	SP1	2.42
		SP5	3.09
P 40 (Slow)	F1	SP1	3.35
		SP5	3.74
	F2	SP1	3.16
		SP5	3.64
	F3	SP1	2.93
		SP5	3.66

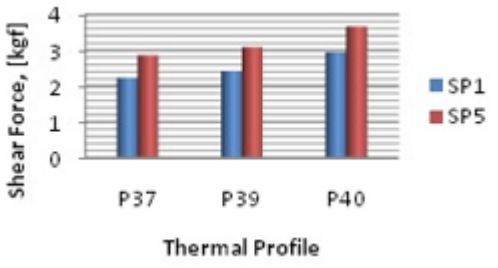

Fig. 6 Comparison between SP1 and SP5 shear force mean values for S1stencil, 0603 chip case and F3 pad finish, for different TP (P37, P39 and P40)

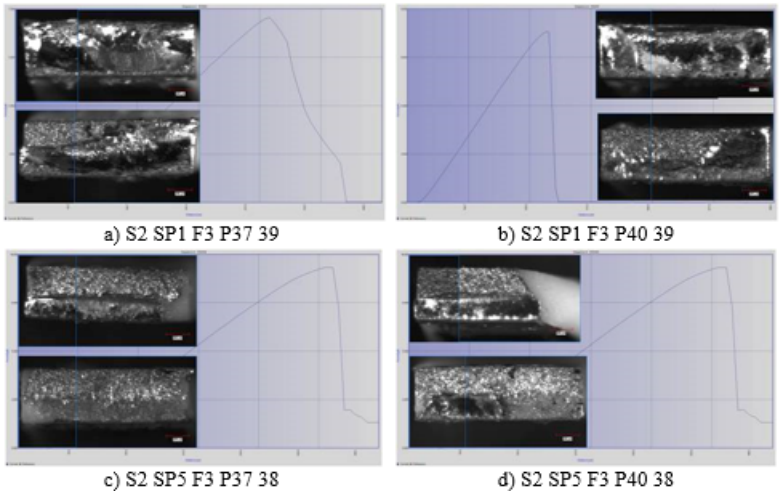

Fig. 7 Shear tests correlation with the solder joint micro stereo fractography for SP1, compare to SP5.

with torsion failure. It's also easy to see that the ductile fraction in SP1 alloy is higher than in SP5 once and in the same time the grain size are in the same rapport in these alloys.

Conclusions

The experiments emphasize the **P**aste influences over solder joints quality having as constants the **P**in-**P**ad-**P**rocess elements of **4P Soldering Model**. The research was focused on analyzing the quality of solder joints realized on special designed test PCBs using different solder paste types and qualities in the same conditions of reflow soldering processes (same TP).

The experiments presented in the paper accomplish the proposed goals by increasing the knowledge concerning VPS process and application. could be A much better design based on the presented experiments will be allowed by further experiments and research.

For the same effort, SN100C resists better than SAC305 to mechanical efforts determined by the thermal fluctuations in the electronic components and circuits plates. Shear tests are in concordance with the stereo micro fractography studies.

From the costs point of view VPS seems to be an ideal solution for SMEs, where production volume is not high. VPS has lower price, does not require too much space for installation, it is easy to install and does not require compressed air and nitrogen. It is necessary only to supply electrical power and water.

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